SysCore3 – A universal Read Out Controller and Data Processing Board*

J. Gebelein[1], *D. Gottschalk*[2], *G. May*[3], *and U. Kebschull*[1]

[1]Infrastructure and Computer Systems for Data Processing (IRI), Frankfurt University, Frankfurt/Main, Germany;
[2]Physikalisches Institut (PI), Heidelberg University, Heidelberg, Germany; [3]GSI, Darmstadt, Germany

The universal SysCore architecture was initially announced in 2007 to provide an optimum balance between fixed requirements and flexibility. The first instance of boards following this principle, acted as development platform for FEE (Front End Electronic), especially the nXYTER with ADC (Analog Digital Converter) and ROC (Read Out Controller). The second slightly modified instance of this board came into operation in several subdetector systems of the CBM experiment, especially as ToF (Time of Flight) ROC where it is used for years now. To extend the usability spectrum, whilst keeping the re-usability approach, a completely new and improved version 3 of the SysCore architecture board has been developed [1]. It allows the CBM collaboration not only to prototype FEE or to develop ROCs, but also to evaluate the DPB (Data Processing Board) capabilities for an optical readout in the CBM service building. In this specific context, the TRD (Transition Radiation Detector) feature extraction is currently an active field of research.

Considering all requirements, such as FMC HPC connectors for high performance connectivity, USB for programming and data transfer, DDR3 for fast memory access, Jitter Cleaner for clock distribution across several boards, optical SFP connectors for CBMnet integration [2] and not to forget an inexpensive central processing FPGA which can be operated in radiation environments, the PCB got a size of 230x230mm. It is made of 16 different layers with a track width/distance of 0,15-0,09mm (micro fine lines). Length compensation for the most critical components such as DDR3, FMC and SFP has been performed. Functional blocks such as power supply, scrubbing controlling or high performance data transfer have been locally combined to provide optimal results. The final board layout can be seen in figure 1.

Programming of the major components on the board can be performed in different ways: The Spartan-6 FPGA itself can be programmed either via USB (Cypress FX2) or JTAG programmer or by the onboard Microsemi ProASIC3 scrubbing controller from a nearby flash memory. The PROASIC3 can be programmed via the Spartan-6 FPGA or a JTAG programmer. This combination allows remote configuration of both FPGAs on the board. Furthermore, the ProASIC3 acts as scrubbing controller for the ToF ROC when it is operated in radiation susceptible environments [3, 4, 5]. This fault tolerance approach has always been a major component of the SysCore architecture and can only by achieved when all components go together. Therefore, the major processing FPGA has been selected to support the background scrubbing feature, the flash memory holding its configuration is a Micron SLC NAND memory with durable charge pumps [6] and the power supply utilizes Linear Technology POL (Point of Load) converters.

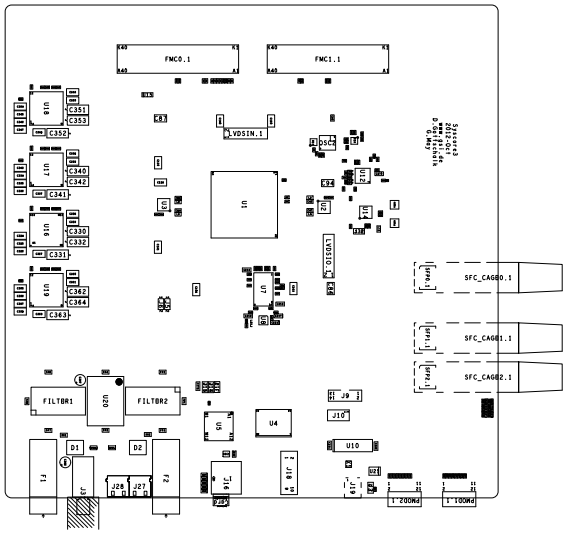

Figure 1: PCB top view of the SysCore3.

References

[1] N. Abel, C. Garcia, J. Gebelein, S. Manz, U. Kebschull, "SysCore3 – a new board for the Universal ROC", CBM Progress Report 2011, Darmstadt, Germany, ISBN 978-3-9811298-9-2

[2] F. Lemke, "Unified Synchronized Data Acquisition Networks", Dissertation, 2012, Mannheim, Germany

[3] N. Abel, H. Engel, J. Gebelein, D. Gottschalk, S. Manz, A. Oancea, U. Kebschull, "Radiation tolerance of the Universal Read Out Controller", CBM Progress Report 2010, Darmstadt, Germany, ISBN 978-3-9811298-8-5

[4] J. Gebelein, H. Engel, U. Kebschull, "FPGA fault tolerance in radiation susceptible environments", Proceedings on Radiation Effects on Components and Systems (RADECS) 2010, Austria

[5] J. Gebelein, U. Kebschull, "Investigation of SRAM FPGA based Hamming FSM encoding in beam test", Proceedings on Radiation Effects on Components and Systems (RADECS) 2012, France

[6] F. Irom, D. N. Nguyen, "Radiation Tests of Highly Scaled High Density Commercial Nonvolatile NAND Flash Memories", JPL TRS, 2011, USA

* Work supported by BMBF (06HD9123I, 06FY7090/05P12RFFCM)