Ten Years of ASIC Design at GSI

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Introduction

In May 2002 the author started to build up an ASIC design group as part of the DVEE department at GSI. Now 10 years later the ASIC design is well established at GSI and has an important role in electronics development for FAIR.

History

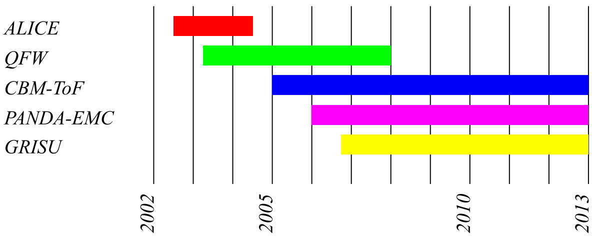

Figure 1: ASIC design projects at GSI since 2002.

The first years have been dominated by setting up the infrastructure and a support of colleagues at the Kirchoff institute of the university of Heidelberg developing readout ASICs for ALICE. As depicted in the time line in figure 1 the first GSI ASIC development started in 2003: the charge to frequency converter QFW[1] which plays now a major role in the beam diagnostics for FAIR.
In 2005 and 2006 the ASIC design group became active in developments for FAIR experiments. The GSI ASIC design started to develop a TDC ASIC for CBM-ToF[3] and a preamplifier and Shaper for PANDA[2]. In 2006 also a program to investigate radiation effects on CMOS semiconductors have been launched[4]. A special test ASIC named GRISU was designed and irradiated in several beam time campaigns.

These projects led into a large number of ASIC tape outs since 2002 as shown in figure 2. The number of designs in UMC 180 nm technology not only contains ASICs designed at GSI but also designs from other collaborators who participate on multi project wafer (MPW) productions financed by GSI. Especially from 2005 to 2008 a lot of developments for the FAIR experiments started which led into a large number of design submissions.
After that a design phase came up with less need of a big number of test structures but a smaller number of large prototype ASICs. In 2012 again a large number of different designs have been taped out.

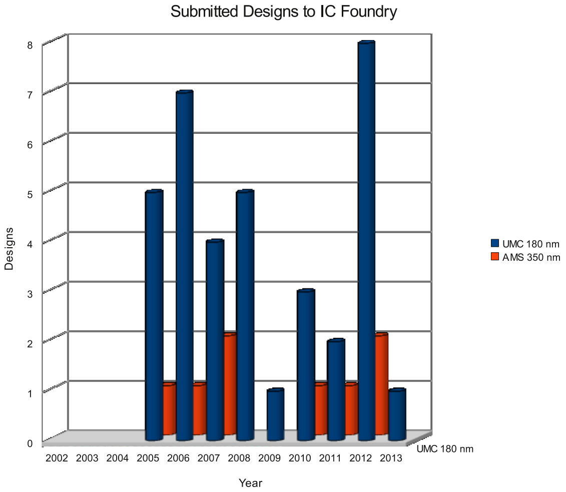

Figure 2: ASIC tape outs since 2002.

Status

The ASIC design group is now a very efficient working group of four designers and one technician. As part of the electronics department there is support from pcb layout and assembly and access to a very well equipped electronics laboratory. For the handling of ASICs the most important equipment like die bonder, wire bonder and prober is available under clean room conditions.
The importance of ASIC design is pointed by the number of ASICs which have to be processed at GSI. Whereas a few years ago only a few prototypes have to be processed for testing in the last years the number increased as more and larger detector modules have to be equipped with ASICs for readout. For 2013 it is expected that more than 1000 ASICs have to be handled at GSI.

References

[1] H. Flemming, E. Badura, “A high dynamic charge to frequency converter ASIC”, GSI Scientific report 2004

[2] P. Wieczorek, H. Flemming, “Low noise preamplifier ASIC for the PANDA EMC”, GSI Scientific report 2006

[3] H. Flemming, H. Deppe, “Development of High Resolution TDC ASICs at GSI”, 2007 IEEE Nuclear Science Symposium Conference Record

[4] S. Löchner, “Radiation Studies on the UMC 180 nm CMOS Process”, GSI Scientific report 2009