

Development of an online feature extraction pre-processing stage for TRD based on SPADIC 1.0 *

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One of the main challenges for the data acquisition of the Transition Radiation Detector (TRD) of the Compressed Baryonic Matter experiment (CBM) is to efficiently process the high data rate produced by the front-end electronics operating in a free streaming data acquisition mode. In this scenario, the TRD detector is read-out by the front-end mixed-signal SPADIC 1.0 chip [1]. The SPADIC 1.0 delivers 32 autonomous read-out channels with a large set of meta-information attached to the generated messages. In order to fulfill the processing requirements for the TRD, a feature extraction online pre-processing stage has been proposed [2]. The aim of the feature extraction is to do an online pre-processing of the front-end electronics data, in order to reduce it by means of parameter extraction and clustering. The Feature Extraction pre-processing stage would be integrated within the functionality of the Data Processing Board (DPB) [3].

As seen in Figure 1, the internal processing logic of the Feature Extraction firmware would allow to instantiate multiple “link processors” in parallel in order to handle the data from different data-input optical links. However, the maximum number of link processors would be constrained by the FPGA resources available.

The internal architecture of the feature extraction core is based on the following processing stages: first, a message interpreter module decodes the incoming SPADIC 1.0 event words wrapped around the CBMnet 2.0 headers and delivers the full timebin RAW data, as well as useful meta-data attached to the hit message (e.g. timestamp, channel id, group id, hit type, etc). This decoded data is then handled by the double-hit detection logic. The double-hit logic works in two configurable modes: first, in conjunction to the double-hit detection logic implemented in the SPADIC 1.0 chip and second, as a stand-alone detection logic. In the first case, the double-hit logic compares the hit-message flags set by the SPADIC 1.0 that tell whether a double-hit was detected or not. In the second case, as a stand-alone detection mode, the logic compares the signal charge with different virtual thresholds at different timebin positions. A parallel running module finds the peaks and valleys in the signal evolution. These information is used by a later logic that splits the message between two maxima, when a valley has been found.

The second processing stage consists mostly of two parallel processes, a total charge integrator (Qtot) and a temporal center of gravity calculator (COG). The Qtot module delivers an amplitude vs. time integration from a region of interest or from all the timebins included in the event. On

the other hand, the COG calculates the center of gravity of the signal in time direction. In order to save FPGA resources, the feature extraction can be configured to use only one of the before mentioned cores. Further beamtest analysis will show which processing module gives better results for the event reconstruction. A final processing stage is called cluster finder and processor. This module finds clusters from events that share similar characteristics, e.g. contiguous fired pads, events with a timestamp that falls within a certain threshold and also by comparing the neighbor trigger matrix flags generated by the SPADIC 1.0. Finally, after a cluster has been completed, the data from each event that belongs to the found cluster is processed by a Center of Gravity (COG) algorithm that provides a temporal resolution of the hit position within the found cluster. In the end, the event building logic wraps the hit-message into CBMnet2.0 containers in order to be shipped to later DPB processing stages.



Figure 1: Block diagram of the internal architecture of the feature extraction core.

Currently, most functionality of the Feature Extraction firmware has been developed and is under continuous testing in a laboratory setup. In 2014, a TRD beamtest will be performed in order to test and provide consistent results about performance and FPGA resource consumption.

References

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- [3] J. Gebelein et al., “SysCore3 A universal Read-Out Controller and Data Processing Board”, CBM Progress Report 2012

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