Further Development of Lattice-FPGA based TDC and Its Implementation on different Platforms

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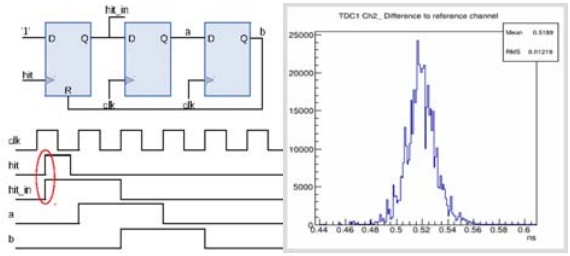
The research on the Lattice ECP3 FPGA based TDC described in [1] was carried out during the year 2013 in order to implement further features (e.g. semi-asynchronous stretcher, calibration trigger) and fix bugs in the design. Moreover, the design was adapted to other readout platforms (e.g. MBS) and implemented on different boards (e.g. FEBEX3, CBMTOF) and several tests were applied to assess the TDC in detail.

Some detectors used in particle physics experiments - e.g. Microchannel Plate (MCP) Detectors used for single photon detection - can generate pulses as short as $1\ ns$. These short signals cannot be measured by the traditional TDL based TDCs, where the state of the start signal has to be preserved until the rising edge of the stop signal, as the falling edge of the start signal would induce another transition in the delay line. In our case the start signal has to conserve the logic high state until the rising edge of the next clock cycle. Therefore, a semi-asynchronous pulse stretcher is designed to extend the length of the hit signals more than one clock period. The stretcher is shown in Figure 1(a).

The stretcher was tested with a $\sim 500\ ps$ wide pulse. In order to measure the width of the short pulse the rising and falling edges of the pulse were measured on two channels. The difference between these two channels was recorded in a histogram after calibration. In Figure 1(b) it can be seen, that the mean of the peak is at $519\ ps$, which gives the width of the pulse. Also the measured precision not considerably deteriorated ($12\ ps$).

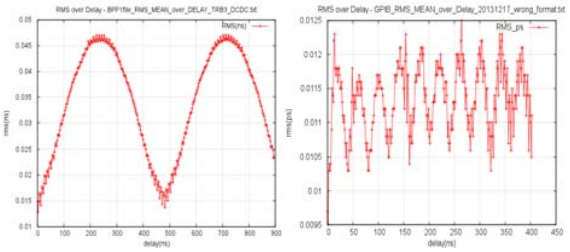
As the delay lines of the TDC channels don't have a constant propagation delay and each of them is unique, they have to be calibrated using random input signals with enough statistics ($\sim\ 10^5$). However, during the experiments it might not be possible to get enough statistics on every channel. Therefore, the TDC was designed to be prompted with a calibration trigger (if supported by the readout platform) to fire every channel with random pulses generated by the on-chip oscillator of the FPGA. After several tests, no deterioration was observed and this unprecise oscillator ($130\ MHz \pm 15\%$ [2]) proved to be an excellent candidate as a random hit generator.

The performance of the TDC was tested for long time intervals between the hit signals (up to $1\ us$). The long time intervals were spawned by using a data timing generator (Tektronix DTG5078) and were measured on two TDC channels on different boards (TRB3, FEBEX3, CBMTOF). In the FPGAs, which are powered by DC-DC converters, a periodic change of the precision over the delay time was discovered. The amplitude of this degradation was recorded as $\sim\ 35\ ps$ (Figure 2(a)). This effect seems to be caused by the noise induced in the supply voltage of the FPGA. In order to test the assumption the DC-DC converters on the board were removed and the test was repeated after the FPGAs were powered with a linear power supply. The peak-to-peak change in the precision over the same delay time was logged as $< 3\ ps$ (Figure 2(b)).



(a) (b)

Figure 1: (a) The falling edge of the input signal is delayed for two clock rising edges. (b) ToT measurement of a $500\ ps$ wide pulse was done on two channels of the TDC with a precision of $12\ ps$.



(a) (b)

Figure 2: The precision change of the TDC over long delay measurements in an FPGA powered by (a) DC-DC converters and (b) linear power supply.

During the July 2013 PANDA Barrel-DIRC Detector Prototype beamtime tests at MAMI-Mainz (Mainzer Mikrotron) the TDC design on TRB3 platform was operated successfully.

References

[1] C. Ugur et.al, "GSI Scientific Report 2012", p.299.

[2] Lattice Semiconductors, "LatticeECP3 Family Handbook", July 2013, HB1009 Version 05.2.

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